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to address this, the accellera□s technical working group (twg) has been working with the ieee-sa and the electronic design automation (eda) forum to develop a new standard on testing electronic design tools. this standard will be published as the ieee 1275 standard for electronic design automation standard test access port and boundary-scan standard test access port, or ieee-1275. this standard defines a common interface for the test access port and boundary scan cell from which standard test vectors can be generated and tested. from the very beginning, standardizing the process of verification has been a main goal for accellera. in order to do this, the top level design module is instantiated within the testbench environment, and design input/output ports are connected with the appropriate testbench component signals. the inputs to the design are driven with certain values for which we know how the design should operate. the outputs are analyzed and compared with the expected values to see if the design behavior is correct. in the end, it is all about the design. it is a strategic decision to spend your time and money on getting the design right or on getting the design right on time. we have many tools that can be used to increase the likelihood of a successful design. these tools are called design □analysis□. by defining a top-level module in the testbench that instantiates the design, all signals of the testbench are connected to the inputs/outputs of the design. input signals are connected to the always blocks of the top-level module, while output signals are connected to the always blocks of the same module. the testbench signal assignments can be changed to create different cases to observe the design behavior.

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all too often, electronic design is approached as a series of isolated disciplines with little knowledge or understanding of the others. the reality is, everything you design has an impact on another part of the design. for example, when designing a digital circuit, you must consider whether the digital clock is coming from a quartz crystal or an oscillator. software toolchains at the center of eda flow are tightly coupled to eda standards and to each other. therefore, software toolchains must be integrated to work together. as we move from the creation of a high-level design to the creation of a manufacturable physical design, the design flow has become more complex. eda verification, however, has always been a challenge. through decades of experience, our eda services organization has developed a variety of techniques to help with various parts of the design flow. from the use of statistical or deterministic simulators to the use of fpgas, our eda services organization can help you make the most of eda tools. these problems exist not only because of the complexity of the designs we are making, but also because of the economics of the semiconductor industry. with moore's law slowing, the industry needs to think about how to make designs smaller, cheaper, and faster. verification is the process of ensuring that a given hardware design works as expected. chip design is a very extensive and time consuming process and costs millions to fabricate. functional defects in the design if caught at an earlier stage in the design process will help save costs. if a bug is found later on in the design flow, then all of the design steps have to be repeated again which will use up more resources, money and time. if the entire design flow has to be repeated, then its called a respin of the chip. 5ec8ef588b